## CLAIMS

What is claimed is:

1. A crossbar switch comprising:

a plurality of master ports, each of the plurality of master ports adapted to interface with a respective one of a plurality of bus masters;

a plurality of slave ports, each of the plurality of slave ports adapted to provide and receive information, at least two of the plurality of slave ports being assigned an overlapping address range to address one or more slave devices; and

control circuitry coupled to the plurality of master ports and the plurality of slave ports, the control circuitry using predetermined arbitration criteria to determine access to the plurality of slave ports when at least one access request to the overlapping address range occurs.

2. The crossbar switch of claim 1 coupled in a data processing system, the data processing system further comprising:

a plurality of slave devices, at least a first portion of the slave devices having multiple ports each of which is coupled to a predetermined different one of the plurality of slave ports and the multiple ports being assigned the overlapping address range.

3. The crossbar switch of claim 2 wherein the data processing system further comprises:

a peripheral coupled to at least one of the plurality of slave devices.

4. The crossbar switch of claim 3 wherein the peripheral is a memory.

5. The crossbar switch of claim 1 coupled in a data processing system, the data processing system further comprising:

a plurality of slave devices, at least a first portion of the slave devices having a single port coupled to a predetermined different one of the plurality of slave ports wherein a first single port is assigned the overlapping

address range with a second single port of the slave devices of the first portion.

6. The crossbar switch of claim 1 wherein the control circuitry further comprises:

a configuration register for storing system operating characteristics for use by the control circuitry to determine a first available slave port when multiple slave ports with the overlapping address range are accessed while being busy.

7. A data processing system, comprising:

a plurality of masters, said plurality of masters including at least a first master and a second master, said first master initiating a first access and said second master initiating a second access;

a slave coupled to said plurality of masters, said slave having a plurality of ports, said plurality of ports including at least a first port and a second port;

shared storage circuitry coupled to said slave, wherein said first port and said second port of said slave access an overlapping address range in said shared storage circuitry; and

an arbiter coupled to said plurality of masters and said slave, said arbiter comprising control circuitry for providing arbitration criteria and wherein said arbiter receives said first access and said second access, and based on said first access, said second access, and said arbitration criteria, selects one of said first port and said second port.

8. The data processing system of claim 7, wherein said arbiter is a crossbar switch and said arbitration criteria provides information comprising at least one of a master priority level, a number of data beats, and a number of wait states per data beat.

9. The data processing system of claim 8, further comprising shared slave port control circuitry which evaluates said number of data beats within an access transaction and said number of wait states per data beat in order to make a determination of slave port availability.

10. The data processing system of claim 7, wherein said overlapping address range is a same address range.

11. The data processing system of claim 7, wherein said arbiter further comprises at least one configuration register, wherein said at least one configuration register indicates which one of said plurality of ports is to be shared by said plurality of masters, provides a non-burst access length for each one of said plurality of masters, provides a size of said memory, provides a number of pages of said memory, and a port wait state for each one of said plurality of ports.

12. The data processing system of claim 11, wherein said port wait state is programmed as dynamic and said arbiter determines said port wait state.

13. The data processing system of claim 7, wherein said control circuitry is programmable.

14. The data processing system of claim 7, wherein said arbiter further comprises:

a plurality of slave port arbiters coupled to said plurality of masters, each one of said plurality of slave port arbiters corresponding to one of said plurality of ports; and

a shared slave port control circuit coupled to said plurality of slave port arbiters, wherein based on said arbitration criteria, said shared slave port control circuit selectively determines which of said plurality of ports is available first.

15. A data processing system, comprising:

a plurality of masters, said plurality of masters initiating multiple access requests;

a slave for being coupled to a peripheral device, said slave having at least a first port and a second port, wherein said first port and said second port use an overlapping address range to address said peripheral device; and

a crossbar switch coupled to the plurality of masters and said slave, said crossbar switch selectively arbitrating for access to said first port and said second port of said slave when said multiple access requests from said plurality of masters occur to said overlapping address range assigned to said peripheral device.

16. The data processing system of claim 15, wherein said overlapping address range is a same address range.

17. The data processing system of claim 15, wherein said slave is a dual port slave.

18. The data processing system of claim 15, wherein said peripheral device is a memory.

19. A method in a data processing system, comprising:

initiating an access to a memory;

determining whether said access is hitting a memory page address that is a currently accessed memory page;

when said access misses a memory page address, determining whether there is an available slave port among a plurality of slave ports associated with a slave;

when there is not an available slave port, determining whether said access is higher in priority than any one of a plurality of current accesses corresponding to said plurality of slave ports;

when said access is higher in priority than any one of said plurality of current accesses, determining whether said access is higher in priority than at least two of said plurality of current accesses; and

when said access is higher in priority than at least two of said plurality of current accesses, determining which one of the at least two of said plurality of current accesses is available first and selecting a slave port corresponding to said one of the at least two of said plurality of current accesses that is available first.

20. The method of claim 19, further comprising:

when said access is hitting said memory page address, steering said access to a port corresponding to said currently accessed memory page.

21. The method of claim 19, further comprising:

when there is said available slave port, steering said access to said available slave port.

22. The method of claim 19, further comprising:

when said access is higher in priority than only one of said plurality of current accesses, steering said access to a slave port corresponding to one of said plurality of current accesses that has a lower priority access that can be arbitrated.

23. The method of claim 19, further comprising:

when said access is a lower priority than any one of said plurality of current accesses, steering said access to a first available slave port based on at least one of a plurality of arbitration criteria, wherein said plurality of arbitration criteria provide criteria indicating at least one of a number of data beats, and a number of wait states per data beat.

24. The method of claim 19, further comprising implementing said slave as a dual port slave.

25. A data processing system, comprising:

a plurality of masters including at least a first master and a second master, said first master initiating a first access and the second master initiating a second access;

a plurality of slave devices including at least a first slave device and a second slave device;

storage circuitry coupled to the first slave device and the second slave device wherein the first slave device and the second slave device access the storage circuitry using an overlapping address range; and

a crossbar switch coupled to the plurality of masters and the plurality of slave devices, the crossbar switch comprising control circuitry for providing arbitration criteria and wherein said crossbar switch receives the first access and the second access, and based on said first access, said second access, and the arbitration criteria, selects one of the first slave device and the second slave device.

26. A method in a data processing system comprising:

initiating an access to a memory;

determining whether said access is hitting a memory page address that is a currently accessed memory page, and if so, steering the access to a same port as the currently accessed page;

when said access misses a memory page address, determining whether there is an available slave port among a plurality of slave ports associated with a slave and steering said access to the available slave port;

when said access is higher in priority than any one of said plurality of current accesses, determining whether said access is higher in priority than at least two of said plurality of current accesses;

when said access is higher in priority than at least two of said plurality of current accesses, determining which one of the at least two of said plurality of current accesses is lowest priority and selecting a slave port corresponding to said one of the at least two of said plurality of current accesses that is lowest priority; and

when said access is not higher in priority than at least two of said plurality of current accesses, steering said access to a slave port having a lowest priority access that can be arbitrated.